Ultra-Small, Low-Power 1KSPS, 16-bit ADC

1 Features

- Wide supply voltage: 2.7V to 5.5V
- Low power consumption: 150uA (continuous conversion mode)
- Programmable data rate: 6.25 SPS to 1K SPS
- Single cycle stable
- Internal low drift voltage reference
- Internal Oscillator
- SPI interface
- Four single-ended inputs or two differential inputs
- Programmable comparator
- Operating temperature range: −40 °C to +125°C

2 Application

- Portable Instruments
- Battery voltage and current monitoring
- Temperature measurement system
- Consumer Electronics
- Factory Automation and Process Control

3 Description

GD30AD3344 device is a SPI -compatible 16-bit high-precision, low-power analog-to-digital converter (ADC) in a small and MSOP-10 package. The GD30AD3344 device integrates a low-drift voltage reference and oscillator. The GD30AD3344 also includes a programmable gain amplifier (PGA) and a digital comparator. These features, combined with a wide operating supply voltage range, make the GD30AD3344 ideal for power -constrained and space-constrained sensor measurement applications.

The GD30AD3344 can perform conversions at data rates up to 1000 samples per second (SPS). The PGA provides an input range from ±64mV to ±6.144V, enabling accurate measurement of large and small signals. The GD30AD3344 has an input multiplexer (MUX) that enables two pairs of differential input measurements or four single-ended input measurements. Digital comparators can be used in the GD30AD3344 for undervoltage and overvoltage detection.

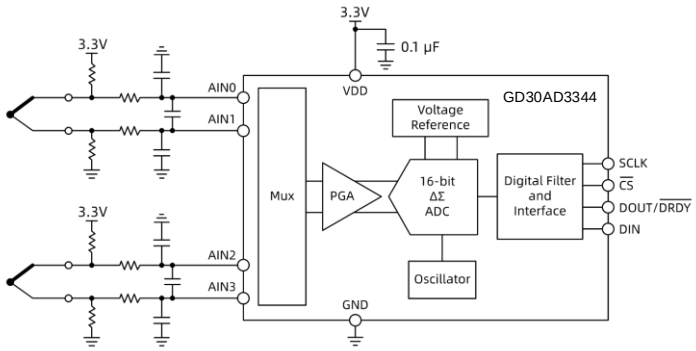
The GD30AD3344 can operate in either continuous conversion mode or single-shot mode. In single-shot mode, these devices automatically power down after one conversion; thus significantly reducing power consumption during idle periods.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
GD30AD3344	MSOP-10	3.00mm x 3.00mm

1. For packaging details, see *Package Information* section.

K- type Thermocouple



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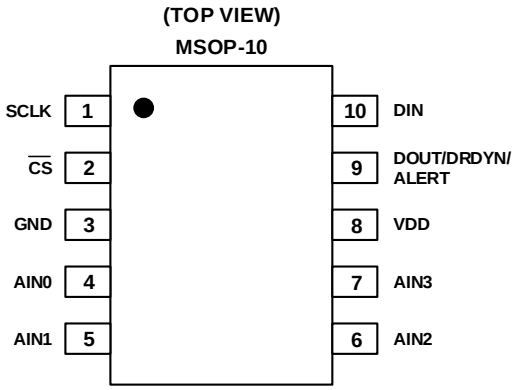
4 Device Overview

4.1 Pinout and Pin Assignment



4.2 Pin Description

PIN NUMBER		PIN TYPE[1]	FUNCTION
NAME	NUM		
SCLK	1	DI	Serial clock input.
$\overline{CS}$	2	D I	Chip Select, active low, if not used, connect to GND .
GND	3	G	Ground.
AIN0	4	AI	Analog Input 0. Leave unconnected or connect to VDD if not used.
AIN1	5	AI	Analog Input 1. Leave unconnected or connect to VDD if not used.
AIN2	6	AI	Analog Input 2. Leave unconnected or connect to VDD if not used.
AIN3	7	AI	Analog Input 3 or Reference Input. Leave unconnected or connect to VDD if not used.
VDD	8	P	Power supply. Connect a 100nF power supply decoupling capacitor to GND.
DOUT / $\overline{DRDY}$	9	DO	Serial data output or data ready, low level is valid.
DIN	10	D I	Serial clock input.

1. P = Power, DI = Digital Input, DO = Digital Output, AI = Analog Input, and GND = Ground.

5 Parameter Information

5.1 Absolute Maximum Ratings

T_A = 25°C, unless otherwise noted[1].

SYMBOL	PARAMETER	MIN	MAX	UNIT
Supply voltage	VDD to GND	−0.3	7	V
Analog input voltage	AIN0, AIN1, AIN2, AIN3	GND − 0.3	VDD + 0.3	V
Digital input voltage	DIN, DOUT / $\overline{DRDY}$, SCLK , $\overline{CS}$	GND − 0.3	VDD + 0.3	V
Continuous input current	Any pin except the power pin	−10	1 0	mA
T_A	Operating temperature	−40	125	°C
T_J	Operating junction temperature	−40	150	°C
T_{stg}	Storage temperature	−60	150	°C

1. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to maximum rated voltage conditions for extended periods may affect device reliability.

5.2 Recommended Operating Conditions

T_A = 25°C, unless otherwise noted.

SYMBOL	PARAMETER	MIN	MAX	UNIT
VDD	VDD to GND	2.7	5.5	V
$V_{(AINP)}$–$V_{(AINN)}$[1]	Full-scale input voltage range[2]	±0.064	±6.144	V
$V_{(AINx)}$[1]	Analog input voltage	GND	VDD	V
V_{DIG}	Digital input voltage	GND	VDD	V
T_A	Operating temperature	−40	125	°C

1. AINP and AINN indicate the selected positive and negative inputs. AINx indicates one of the four available analog inputs.
2. This parameter represents the full-scale input voltage range of the ADC scaling. The analog inputs of the device cannot exceed VDD + 0.3V.

5.3 ESD Performance

SYMBOL	CONDITIONS	VALUE	UNIT
$V_{ESD(HBM)}$	Human-body model (HBM), ANSI/ESDA/JEDEC JS-001-2017[1]	±2000	V
$V_{ESD(CDM)}$	Charge-device model (CDM), ANSI/ESDA/JEDEC JS-002-2022[2]	±500	V

1. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing using standard ESD control processes.
2. JEDEC document JEP157 states that a 250-V CDM allows safe manufacturing using standard ESD control processes.

5.4 Thermal Resistance

SYMBOL[1]	CONDITIONS	MSOP-10	UNIT
Θ_{JA}	Junction to ambient thermal resistance	182.7	°C/W
$\Theta_{JC\ (TOP)}$	Junction to case (top) thermal resistance	67.2	°C/W
Θ_{JB}	Junction to board thermal resistance	103.8	°C/W
Ψ_{JB}	Junction-to-Board Parameters	102.1	°C/W
Ψ_{JT}	Junction to Top Parameters	10.2	°C/W

1. Thermal resistance characteristic parameter data is based on thermal simulation results and complies with JEDEC document JESD51-7.

5.5 Technical Specifications

VDD = 3.3 V, data rate = 6.25 SPS, full-scale input voltage range (FSR) = ±2.048 V (unless otherwise noted). Maximum and minimum specifications apply for T_A = −40 °C to +125 °C. Typical specifications are for T_A = 25 °C.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Analog input impedance			1		GΩ
System Performance					
Resolution (no missing code)		16			Bits
Data Rate (DR)		6.25, 12.5, 25, 50, 100, 250, 500, 1000			SPS
Data rate changes	All data rates	−5		5	%
Output Noise		See the *Noise Performance* section			
Integral Nonlinearity (INL)	DR = 6.25SPS, FSR = ±2.048V[2]		10		ppm/ FSR
Offset Error	FSR = ±2.048 V, differential input		±0.1	±2	LSB
	FSR = ±2.048 V, single-ended input		±0.25		
Temperature offset drift	FSR = ±2.048 V		0.005		LSB /°C
Long term offset drift	FSR = ±2.048 V, T_A = 125°C, 1000hrs		±1		LSB
Offset Power Supply Rejection	FSR = ±2.048 V, DC supply variation		1		LSB / V
Offset Channel Matching	A match between any two inputs		3		LSB
Gain Error[3]	FSR = ±2.048 V, TA = 25°C		0.1	0.2	%
Gain drift with temperature[3]	FSR = ±0.256 V		10		ppm/°C
	FSR = ±2.048 V		10	40	ppm/°C
	FSR = ±6.144 V[1]		10		ppm/°C
Long-term gain drift[3]	FSR = ±2.048 V, T_A = 125°C, 1000hrs		±0.05		%
Gain Power Supply Rejection			40		ppm /V
Gain Match[3]	Matching between any two gains		0.02	0.1	%
Gain channel matching	A match between any two inputs		0.05	0.1	%

Technical Specifications (Continued)

VDD = 3.3 V, data rate = 6.25 SPS, full-scale input voltage range (FSR) = ±2.048 V (unless otherwise noted). Maximum and minimum specifications apply for T_A = −40 °C to +125 °C. Typical specifications are for T_A = 25°C.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Common Mode Rejection Ratio(CMRR)	at DC, FSR = ±0.256V		105		dB
	at DC, FSR = ±2.048V		100		dB
	at DC, FSR = ±6.144V [1]		90		dB
	f_{CM} = 60Hz, DR = 6.25SPS		105		dB
	f_{CM} = 50Hz, DR = 6.25SPS		105		dB
Digital Input/Output					
High level input voltage (VIH)		0.7VDD		VDD	V
Low level input voltage (V_{LH})		GND		0.3VDD	V
Low level output voltage (V_{OL})	I_{OL} = 3mA	GND	0.15	0.4	V
Input leakage current	GND < VDIG < VDD	−10		10	μA
Power Supply					
Supply Current (I_{VDD})	Power-down mode, T_A = 25°C		0.5	2	μA
	Power-down mode			5	
	Operating mode, T_A = 25°C		150	200	
	Working Mode			300	
consumption (PD)	VDD = 5.0V		0.9		mW
	VDD = 3.3V		0.5		
	VDD = 2.7V		0.3		

1. This parameter represents the full -scale range of the ADC scaling. The voltage applied to the analog input does not exceed VDD + 0.3V.
2. Best fit INL; covers 99% of full scale.
3. Includes all errors from the PGA and voltage reference.

5.6 SPI Timing Specifications

Over the operating ambient temperature range and VDD = 2.7 V to 5.5 V (unless otherwise noted).

		MIN	MAX	UNIT
t_{CSSC}	Delay time, $\overline{CS}$ falling edge to first SCLK rising edge[1]	100		ns
t_{SCCS}	Delay time, the final SCLK falling edge to $\overline{CS}$ rising edge	100		ns
t_{CSH}	Pulse duration, $\overline{CS}$ high	200		ns
t_{SCLK}	SCLK period	250		ns
t_{SPWH}	Pulse duration, SCLK high	100		ns

SPI Timing Specifications(Continued)

Over the operating ambient temperature range and VDD = 2.7V to 5.5V (unless otherwise noted).

		MIN	MAX	UNIT
t_{SPWL}	Pulse duration, SCLK low[2]	100		ns
			28	ms
t_{DIST}	Setup time, DIN valid before SCLK falling edge	50		ns
t_{DIHD}	Hold time, DIN valid after SCLK falling edge	50		ns
t_{DOHD}	Hold time, SCLK rising edge to DOUT invalid	0		ns

1. If the serial bus is not shared with any other device, it $\overline{CS}$ can be pulled low permanently .
2. Holding SCLK low for more than 28 ms resets the SPI interface.

Timing requirements

PARAMETER	CONDITIONS	MIN	MAX	UNIT
Propagation delay time, $\overline{CS}$ falling edge to DOUT driver	DOUT load = 20pF100kΩ to GND		100	ns
Propagation delay time, SCLK rising edge to valid new DOUT	DOUT load = 20pF100kΩ to GND	0	50	ns
Propagation delay time, $\overline{CS}$ rising edge to DOUT high impedance	DOUT load = 20pF100kΩ to GND		100	ns

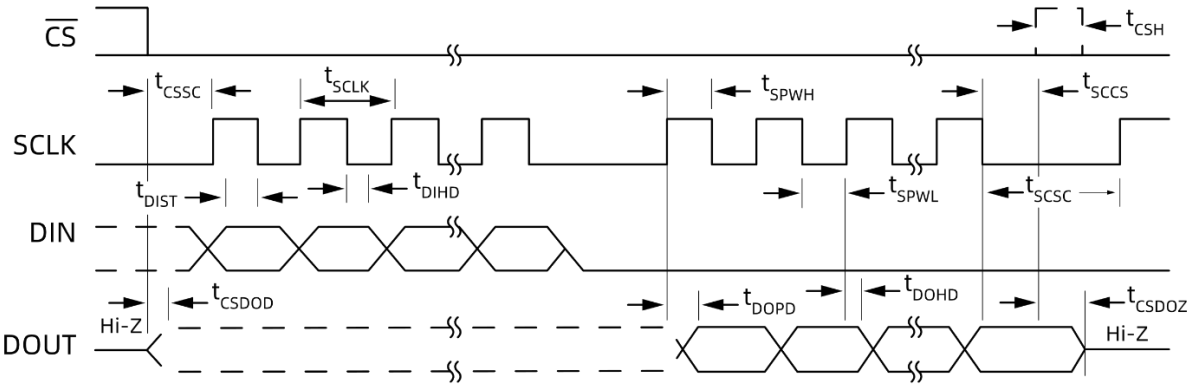


Figure 1. SPI Interface Timing

6 Parameter Measurement Information

6.1 Noise Performance

Delta-sigma analog-to-digital converters (ADCs) are based on the principle of oversampling. The input signal to a delta-sigma ADC is sampled at a high frequency (the modulator frequency) and subsequently filtered and decimated in the digital domain to produce a conversion result at the corresponding output data rate. The ratio between the modulator frequency and the output data rate is called the oversampling ratio (OSR). By increasing the OSR, and thus reducing the output data rate, the noise performance of the ADC can be optimized. In other words, when the output data rate is reduced, the input referred noise decreases because more samples of the internal modulator are averaged to produce one conversion result. Increasing the gain can also reduce the input referred noise, which is particularly useful when measuring low-level signals.

Table 1 and Table 2 summarize the noise performance of the GD30AD3344. The data represent typical noise performance at T_A = 25 °C with the inputs shorted together externally. The input referred noise in μVRMS under the conditions shown in Table 1. Note that the μVPP values are shown in parentheses. Table 2 shows the effective resolution calculated from the μVRMS values using Equation(1). The noise-free resolution calculated from the peak-to-peak noise values using Equation(2)

$$\text{Effective Resolution} = \ln(FSR / V_{RMS\_Noise}) / \ln 2 \quad (1)$$

$$\text{Noise-Free Resolution} = \ln(FSR / V_{PP\_Noise}) / \ln 2 \quad (2)$$

Table 1. Noise in uV_{RMS} (uV_{PP}) at VDD = 3.3V

Data Rate (SPS)	FSR (Full-Scale Range)						
	±6.144 V	±4.096 V	±2.048 V	±1.024 V	±0.512 V	±0.256 V	±0.064 V
6.25	187.5 (187.5)	125 (125)	62.5 (62.5)	31.25 (31.25)	15.62 (15.62)	7.81 (7.81)	1.95 (1.95)
12.5	187.5 (187.5)	125 (125)	62.5 (62.5)	31.25 (31.25)	15.62 (15.62)	7.81 (7.81)	1.95 (1.95)
25	187.5 (187.5)	125 (125)	62.5 (62.5)	31.25 (31.25)	15.62 (15.62)	7.81 (7.81)	1.95 (1.95)
50	187.5 (187.5)	125 (125)	62.5 (62.5)	31.25 (31.25)	15.62 (15.62)	7.81 (7.81)	1.95 (1.95)
100	187.5 (187.5)	125 (125)	62.5 (62.5)	31.25 (31.25)	15.62 (15.62)	7.81 (7.81)	1.95 (1.95)
250	187.5 (187.5)	125 (125)	62.5 (62.5)	31.25 (31.25)	15.62 (15.62)	7.81 (7.81)	1.95 (1.95)
500	187.5 (187.5)	125 (125)	62.5 (62.5)	31.25 (31.25)	15.62 (15.62)	7.81 (7.81)	1.95 (2.63)
1000	187.5 (187.5)	125 (125)	62.5 (62.5)	31.25 (31.25)	15.62 (15.62)	7.81 (7.81)	1.95 (3.77)

Table 2. Effective Resolution (Noise-Free Resolution) When VDD = 3.3V

Data Rate (SPS)	FSR (Full-Scale Range)						
	±6.144 V	±4.096 V	±2.048 V	±1.024 V	±0.512 V	±0.256 V	±0.064 V
6.25	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)
12.5	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)
25	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)
50	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)
100	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)
250	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)
500	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (15.57)
1000	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (15.04)

7 Detailed Description

7.1 Module Block Diagram

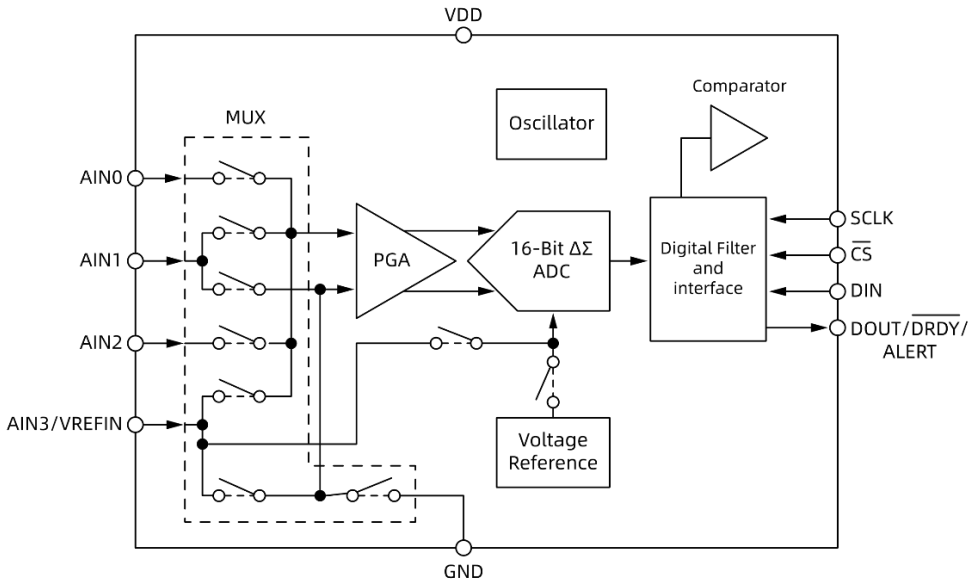


Figure 2. GD30A3344 Block Diagram

7.2 Operation

7.2.1 Overview

The GD30AD3344 is a very small, low-power 16-bit delta-sigma analog-to-digital converter (ADC). The GD30AD3344 contains a delta-sigma ADC core with an internal voltage reference, a clock oscillator, and an SPI interface. The GD30AD3344 also integrates a programmable gain amplifier (PGA) and a programmable digital comparator. Figure 2 shows the functional block diagram of the GD30AD3344 .

GD30AD3344 ADC core measures the differential signal VIN, which is the difference between V(AINP) and V(AINN). The converter core consists of a differential switched capacitor delta-sigma modulator and a digital filter. The input signal is compared with an internal reference voltage. The digital filter receives a high-speed bit stream from the modulator and outputs data proportional to the input voltage.

The GD30AD3344 has two available conversion modes: single mode and continuous conversion mode. In single mode, the ADC performs one conversion on the input signal upon request, stores the conversion value to the internal conversion register, and then enters a power-down state. This mode is designed to provide significant power savings for systems that only require periodic conversions or have long idle times between conversions. In continuous conversion mode, the ADC automatically starts conversion of the input signal as soon as the previous conversion is completed. The rate of continuous conversion is equal to the programmed data rate. Data can be read at any time and reflects the completed conversion in real time.

7.3 Features

7.3.1 Multiplexer

The GD30AD3344 contains an input multiplexer (MUX), as shown in Figure 3. Four single-ended signals or two differential signals can be measured. In addition, AIN0 and AIN1 may be measured differentially with AIN3. The multiplexer is configured by the MUX[2:0] bits in the Config register. When measuring single-ended signals, the negative input of the ADC is connected to GND through a switch inside the multiplexer.

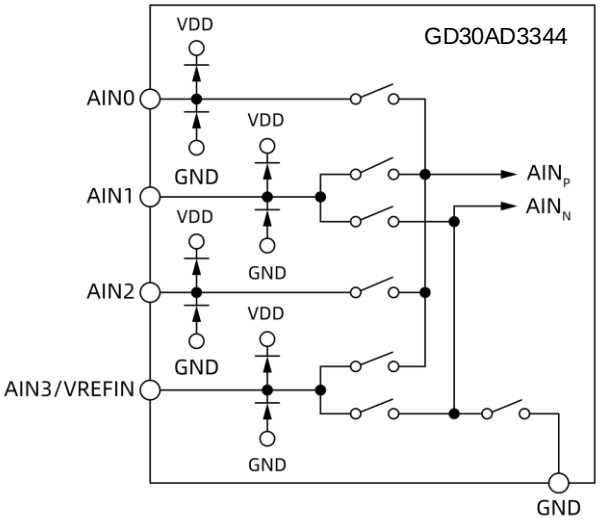


Figure 3. Input Multiplexer

When measuring single-ended inputs, the device does not output negative codes. These negative codes represent negative differential signals, that is, (V(AINP) - V(AINN)) < 0. Electrostatic discharge (ESD) diodes connected to VDD and GND protect the GD30AD3344 analog inputs. Keep the absolute voltage of any input form within the range shown in Equation(3) to prevent the ESD diodes from turning on.

$$GND - 0.3V < V_{(AINX)} < VDD + 0.3V \quad (3)$$

If the voltage on the input pin violates these conditions, use an external Schottky diode and series resistor to limit the input current to a safe value (see the *Absolute Maximum Ratings*).

7.3.2 Analog Input

The GD30AD3344 input front end integrates a high-impedance input programmable gain amplifier to greatly reduce input current, with a typical input impedance of 1GΩ.

7.3.3 Full Scale Range (FSR) and LSB Size

A programmable gain amplifier (PGA) is implemented before the delta-sigma ADC of the GD30AD3344. The full-scale range is configured by the PGA [2: 0] bits in the Config register and can be set to ±6.144 V, ±4.096 V, ±2.048 V, ±1.024 V, ±0.512 V, ±0.256 V, ±0.064 V. Table 3 shows the FSR and the corresponding LSB size. Equation(4) shows how to calculate the LSB size from the selected full-scale range.

$$LSB = FSR / 2^{16} \quad (4)$$

Table 3. Full-Scale Range and Corresponding LSB Size

Full scale range	The size of the least significant bit
±6.144 V [1]	187.5 μV
±4.096 V [1]	125 μV
±2.048 V	62.5 μV
±1.024 V	31.25 μV
±0.512 V	15.625 μV
±0.256 V	7.8125 μV
±0.064 V	1.9531 μV

1. This parameter represents the full-scale range of the ADC scaling. Do not apply voltages exceeding VDD + 0.3 V to the analog inputs of the device.

The analog input voltage must not exceed the analog input voltage limits given in *Absolute Maximum Ratings*. If a VDD supply voltage greater than 4 V is used, the ± 6.144 V full-scale range allows the input voltage to extend to the supplies. Although in this case (or when the supply voltage is less than the full-scale range; for example, VDD = 3.3 V and the full-scale range = ±4.096 V), the full-scale ADC output value cannot be obtained. For example, when VDD = 3.3 V and FSR = ±4.096 V, only signals up to VIN = ±3.3 V can be measured, which in this case results in a loss of part of the measurement dynamic range.

7.3.4 Reference Voltage

The GD30AD3344 integrates a voltage reference. Errors associated with initial voltage reference accuracy and reference drift over temperature are included in the gain error and gain drift specifications in the electrical characteristics table.

Supports AIN 3 as an external reference source.

7.3.5 Oscillator

The GD30AD3344 has an integrated oscillator that runs at 512 kHz. No external clock is required to operate these devices. The internal oscillator drifts with temperature and time. The output data rate is proportional to the oscillator frequency.

7.3.6 Output Data Rate and Conversion Time

The GD30AD3344 provides programmable output data rates. Use the DR [2:0] bits in the Config register to select output data rates of 6.25 SPS, 12.5 SPS, 25 SPS, 50 SPS, 100 SPS, 250 SPS, 500 SPS, or 1000 SPS.

The GD30AD3344 is stable within one cycle; therefore, the conversion time is equal to 1 / DR.

7.4 Functional Mode

7.4.1 Reset and Power-On

The GD30AD3344 is reset at power-on and sets all bits in the Config register to their respective default settings. The GD30AD3344 enters a power-off state after completing the reset process. The device interface and digital blocks are active, but no data conversion is performed. The initial power-off state of the GD30AD3344 can alleviate power-critical systems from experiencing surges during power-on.

7.4.2 Operation Mode

The GD30AD3344 operates in one of two modes: continuous conversion mode or single-shot mode. The corresponding operation mode can be selected by the MODE bit in the Config register.

7.4.2.1 Single Mode

When the MODE bit in the Config register is set to 1, the GD30AD3344 enters a power-down state and operates in single-shot mode. This power-down state is the default state when the GD30AD3344 is first powered on. The device will respond to commands despite being powered off. The GD30AD3344 will remain in this power-down state until a 1 is written to the operating status (OS) bit in the Config register. When the OS bit is set, the device powers up in approximately 25 μs, resets the OS bit to 0, and begins a single conversion. When the data conversion is complete, the device powers down again. Writing a 1 to the OS bit while a conversion is in progress has no effect. To switch to continuous conversion mode, write a 0 to the MODE bit in the Config register.

7.4.2.2 Continuous Conversion Mode

In continuous conversion mode (MODE bit set to 0), the GD30AD3344 performs conversions continuously. After the conversion is completed, the GD30AD3344 places the result into the conversion register and immediately starts another conversion.

When programming new configuration settings, the conversion currently in progress is completed using the previous configuration settings. Thereafter, continuous conversions using the new configuration settings begin. To switch to single conversion mode, write a 1 to the MODE bit in the configuration register or reset the device.

7.4.3 Low Power Consumption Duty Cycle

A delta-sigma ADC generally improves when the output data rate is reduced because more samples of the internal modulator are averaged to produce one conversion result. In applications where power consumption is critical, the improved noise performance at low data rates may not be necessary. For these applications, the GD30AD3344 supports duty cycles, which significantly saves power by periodically requesting high data rate readings at an effectively lower data rate. For example, the power consumption of the GD30AD3344 set by the host controller at a data rate of 1000 SPS is 1/125 of the power consumption at a data rate of 8 SPS, because the conversion at a rate of 1000 SPS only takes about 1ms, and the conversion at a rate of 8 SPS takes about 125 ms, so that 8SPS will work 124 ms more than 1000 SPS. The host controller can arbitrarily define the sampling duty cycle. The GD30AD3344 provides lower data rates and also provides improved noise performance when needed.

7.5 Programming

7.5.1 SPI interface

The SPI-compatible serial interface consists of four signals ($\overline{CS}$, SCLK , DIN and DOUT / $\overline{DRDY}$) or three signals (in this case $\overline{CS}$ directly connected to low level). This interface is used to read conversion data, read and write registers, and control device operation.

7.5.2 Chip Select

The chip select pin ($\overline{CS}$) selects the GD30AD3344 for SPI communication. This feature is useful when multiple devices share the same serial bus. It is held $\overline{CS}$ low during serial communication . When $\overline{CS}$ pulled high, the serial interface is reset, SCLK is ignored, and DOUT / $\overline{DRDY}$ enters a high-impedance state. In this state, DOUT / $\overline{DRDY}$ no data-ready indication is provided . In the presence of multiple devices, it must be monitored DOUT / $\overline{DRDY}$ and periodically lowered $\overline{CS}$. At this point, the pin DOUT / $\overline{DRDY}$ either immediately goes high, indicating that no new data is available, or immediately goes low, indicating that new data is present in the conversion register and is available for transmission. New data can be transmitted at any time without worrying about data corruption. When the transmission begins, the current result is locked into the output shift register and does not change until the communication is completed. This system avoids any possibility of data corruption.

7.5.3 Serial Clock

The serial clock (SCLK) has a Schmitt trigger input and is used to clock the data in and out of the DIN and DOUT / $\overline{DRDY}$ GD30AD3641. Even though the input has hysteresis, it is recommended to keep SCLK as clean as possible to prevent glitches from accidentally moving data. If SCLK is held low for 28 ms, the serial interface is reset and the next SCLK pulse starts a new communication cycle. This timeout feature can be used to resume communication when a serial interface transmission is interrupted. When the serial interface is idle, keep SCLK low.

7.5.4 Data Entry

The data input pin (DIN) is used with SCLK to send data to the GD30AD3344. The device latches data on DIN on the falling edge of SCLK. The GD30AD3344 never drives the DIN pin.

7.5.5 Data Out and Data Ready

The data out and data ready pins (DOUT / $\overline{DRDY}$ active low) are used with SCLK to read conversion and register data from the GD30AD3344. DOUT / $\overline{DRDY}$ data on the GD30AD3344 is shifted out on the rising edge of SCLK. It is also used to indicate that the conversion is complete and new data is available. The pin DOUT / $\overline{DRDY}$ goes low when new data is ready. DOUT / $\overline{DRDY}$ can also trigger the microcontroller to start reading data from the GD30AD3344. In continuous conversion mode, if no data is read from the device , DOUT / $\overline{DRDY}$ goes high again 8μs before the next data ready signal (DOUT / $\overline{DRDY}$ active low). This transition is shown in the figure below. The data transfer is completed before DOUT / $\overline{DRDY}$ returning high.

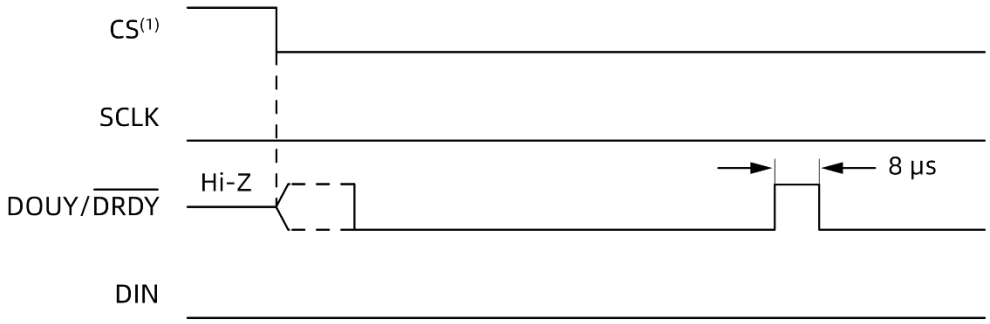


Figure 4. Schematic Diagram of Continuous Conversion Mode without Data DOUT / $\overline{DRDY}$ Reading

When $\overline{CS}$ high, the default configuration of DOUT / $\overline{DRDY}$ has a weak internal pull-up resistor. This feature reduces the risk of DOUT / $\overline{DRDY}$ floating near the middle of the supply and causing leakage current in the master device . To disable this pull-up resistor and put the device in a high-impedance state, set the PULL_UP_EN bit in the configuration register to 0.

7.5.6 Data Format

The GD30AD3344 provides 16-bit data in two's complement format. A positive full-scale (+FS) input produces an output code of 7FFFh, and a negative full-scale (–FS) input produces an output code of 8000h. For signals exceeding full-scale, data up to full-scale is displayed. Table 4 summarizes the ideal output codes for different input signals. The following figure shows the relationship between code transition and input voltage.

Table 4. Input Signals and Ideal Output Codes

Input Signal ($V_{INAINPAINN}$)	Ideal Output Code[1]
≥ +FS ($2^{15} - 1$)/2^{15}	7FFF
+FS/2^{15}	0001h
0	0000h
–FS/2^{15}	FFFFh
≤ –FS	8000h

1. Does not include the effects of noise, INL, offset, and gain errors.

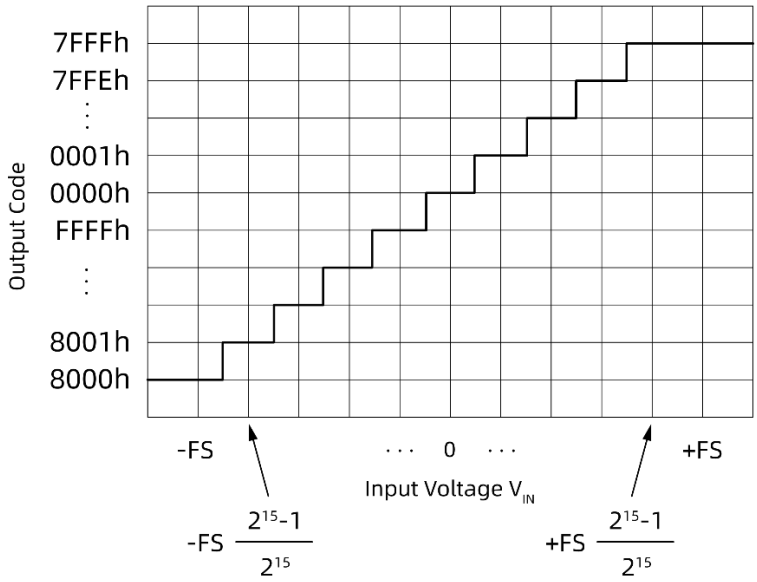


Figure 5. Code Conversion Diagram

7.5.7 Data Reading

For single and continuous conversion modes, data is written and read from the GD30AD3344 in the same way, without issuing any commands. The operating mode of the GD30AD3344 is selected by the MODE bit in the Config register.

The device can be placed in continuous conversion mode by setting the MODE bit to 0. In continuous conversion mode, the device $\overline{CS}$ continuously initiates new conversions even when OUT is high .

For single-shot mode, set the MODE bit to 1. In single-shot mode, a new conversion is started simply by writing a 1 to the SS bit. Conversion data is always buffered, and the current data is retained until it is replaced by new conversion data. Therefore, data can be read at any time without worrying about data corruption. When DOUT / $\overline{DRDY}$ set low, it indicates that new conversion data is ready, and the conversion data is read by shifting the data out . The MSB (15th bit) of the upper data in the DOUT / $\overline{DRDY}$ is output on the first SCLK rising edge. While the conversion result is being output from the DOUT / $\overline{DRDY}$, the new configuration register data is latched

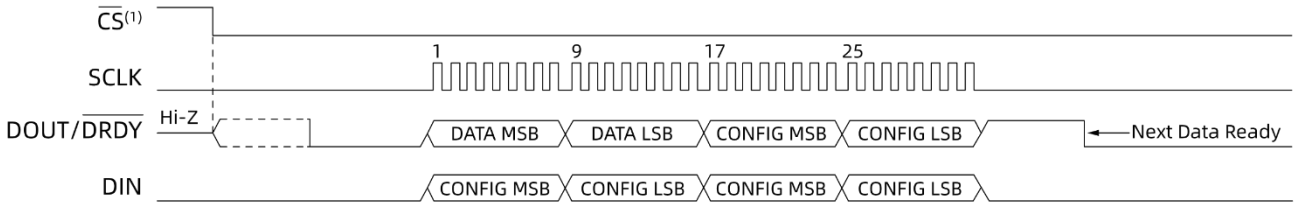
onto DIN on the SCLK falling edge.

GD30AD3344 also offers the possibility to directly read back the configuration register settings within the same data transfer cycle. A complete data transfer cycle consists of 32 bits (when using Config register data readback) or 16 bits (only used when the line can be controlled and is not permanently pulled low).

7.5.8 32- Bit Data Transmission Cycle

The data in a 32-bit data transfer cycle consists of four bytes: two bytes for the conversion result and two bytes for configuration register readback. The device always reads the MSB first.

Write the same Config register setting twice in one transfer cycle, as shown in the following figure. If convenient, write the Config register setting once in the first half of the transfer cycle, and then hold the DIN pin low or high in the second half of the cycle. If the configuration register does not need to be updated, hold the DIN pin low or high throughout the transfer cycle. The Config register setting written in the first two bytes of a 32-bit transfer cycle is read back in the last two bytes of the same cycle.



1. If the GD30AD3344 is not sharing the serial bus with other devices , it $\overline{CS}$ can be held low. If $\overline{CS}$ it is low, DOUT / $\overline{DRDY}$ asserting low indicates that new data is available

Figure 6. 32-Bit Data Transfer Cycle for Configuration Register Readback

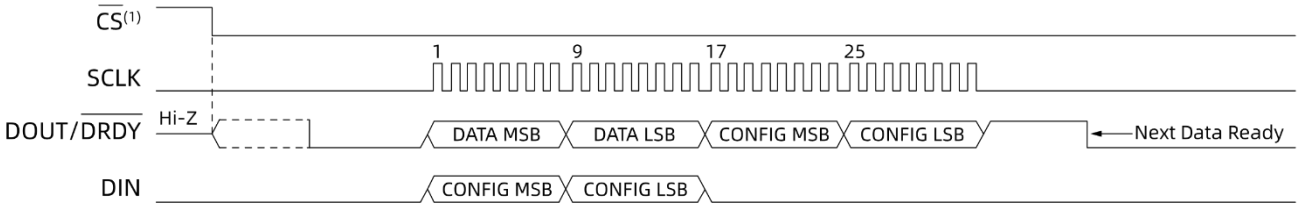


Figure 7. 32-Bit Data Transmission Cycle DIN Remains Low

7.5.9 16-Bit Data Transfer Cycle

If the configuration register data does not need to be read back, the GD30AD3344 conversion data can also be output in a shorter 16 -bit data transfer cycle, as shown in the figure below. Therefore, it must be pulled $\overline{CS}$ high after the 16th SCLK cycle. Pulling the pin $\overline{CS}$ high resets the SPI interface. The next time $\overline{CS}$ is pulled low, data transfer starts with the currently buffered conversion result at the first SCLK rising edge. If the pin DOUT / $\overline{DRDY}$ is low at the beginning of the data read , the conversion buffer has been updated with the new result. Otherwise , if DOUT / $\overline{DRDY}$ is high, the same result of the previous data transfer cycle is read.

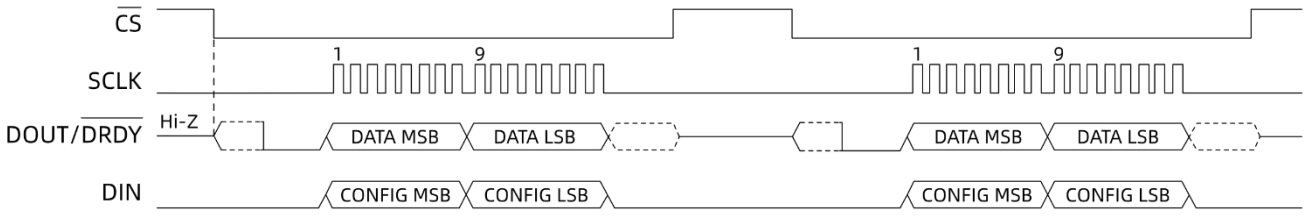


Figure 8. 16-Bit Data Transmission

7.6 Register Map

The GD30AD3344 has two registers. The conversion register contains the result of the last conversion. The configuration register is used to change the operating mode of the GD30AD3344 and query the status of the device.

7.6.1 Conversion Register (P[1:0]=0h) [Reset=0000h]

The 16-bit conversion register contains the result of the last conversion in two's complement format. After power-up, the conversion register is cleared to 0 and remains at 0 until the first conversion is completed.

Table 5. Conversion Registers

15	14	13	12	11	10	9	8
D15	D14	D13	D12	D11	D10	D9	D8
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
D7	D6	D5	D4	D3	D2	D1	D0
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

Example: RW = read-write; R = read-only; -n = reset value

Table 6. Conversion Register Field Description

Bit	Fields	type	Reset value	Description
15:0	D[15:0]	R	0000h	16-bit conversion result

7.6.2 Configuration Register (Config Register) (P[1:0]=1h)[Reset = 058Bh]

The 16-bit configuration register can be used to control the GD30AD3344 operating mode, input selection, data rate, and full- scale range.

Table 7. Configuration Registers

15	14	13	12	11	10	9	8
OS	M UX[2:0]			P GA[2:0]			MODE
R/W-0h	R/W-0h			R/W-2h			R/W-1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DR [2:0]			Reserved	PULL_UP_EN	NOP [1:0]		Reserved
R/W-4h			R/W-0h	R/W-1h	R/W-1h		R/W-1h

Example: RW = read-write; R = read-only; -n = reset value

Table 8. Configuration Register Field Description

Bit	Field	Type	Reset	Description
15	OS	R/W	0h	**Run state or single conversion start** This bit determines the operating state of the device. The OS can only write to it in the power-down state and has no effect while a conversion is in progress. When writing: 0 = Invalid

Bit	Field	Type	Reset	Description
				1 = Start a single conversion (in power-down state) Always reads back 0 (default).
14:12	MUX[2:0]	R/W	0h	**Input Multiplexer Configuration** These bits configure the input multiplexe . 000 = AINP is AIN0 and AINN is AIN1 (default) 001 = AINP is AIN0 and AINN is AIN3 010 = AINP is AIN1 and AINN is AIN3 011 = AINP is AIN2 and AINN is AIN3 100 = AINP is AIN0 and AINN is GND 101 = AINP is AIN1 and AINN is GND 110 = AINP is AIN2 and AINN is GND 111 = AINP is AIN3 and AINN is GND
11:9	PGA[2:0]	R/W	2h	**Programmable Gain Amplifier Configuration** These bits set the FSR of the programmable gain amplifier. 000 = FSR = ±6.144V1 001 = FSR = ±4.096V1 010 = FSR = ±2.048V (default) 011 = FSR = ±1.024V 100 = FSR = ±0.512 V 101 = FSR = ±0.256 V 110 = FSR = ±0.064V
8	MODE	R/W	1h	**Device operation mode** This bit controls the operating mode of the GD30AD3344. 0 = Continuous conversion mode 1 = Power-down and one-shot mode (default)
7:5	DR [2:0]	R/W	4h	**Data Rate** These bits control the data rate setting. 000 = 6.25SPS 001 = 12.5SPS 010 = 25SPS 011 = 50SPS 100 = 100SPS (default) 101 = 250SPS 110 = 500SPS 111 = 1000SPS
4	Reserved	R/W	0h	**Reserved** Writing 0 or 1 to this bit has no effect.
3	PULL_UP_EN	R/W	1h	DOUT / $\overline{\text{DRDY}}$ **Pin pull-up function enable bit** When high DOUT / $\overline{\text{DRDY}}$ only , this bit enables $\overline{\text{CS}}$ the weak internal pull-up resistor on the pin. When enabled, the internal 400-kΩ resistor connects the bus line to the supply. When disabled, DOUT / $\overline{\text{DRDY}}$ the pin floats.

Bit	Field	Type	Reset	Description
				0 = Disable pull-up resistor on pin DOUT / $\overline{DRDY}$ 1 = Enable pull-up resistor on pin (default) DOUT / $\overline{DRDY}$
2:1	NOP [1:0]	R/W	1h	**No operation** The NOP [1:0] bits control whether data is written to the configuration register. For data to be written to the configuration register, the NOP [1:0] bits must be “01”. Any other value results in a NOP command. DIN can be held high or low during the SCLK pulse without data being written to the configuration register. 00 = Invalid data, do not update the contents of the Config register 01 = Valid data, Update Conf ig register (default) 10 = Invalid data, do not update the contents of the Config register 11 = Invalid data, do not update the content configuration register
0	Reserved	R	1h	**Reserved** Writing 0 or 1 to this bit has no effect. Always reads back 1.

1. This parameter represents the full-scale range of the ADC scaling. Do not apply voltages exceeding VDD+0.3V to the ADC.

8 Application and Implementation

Example circuits and suggestions for using the GD30AD3344 in various situations.

8.1 SPI Basic Connection

As shown in Figure 9:

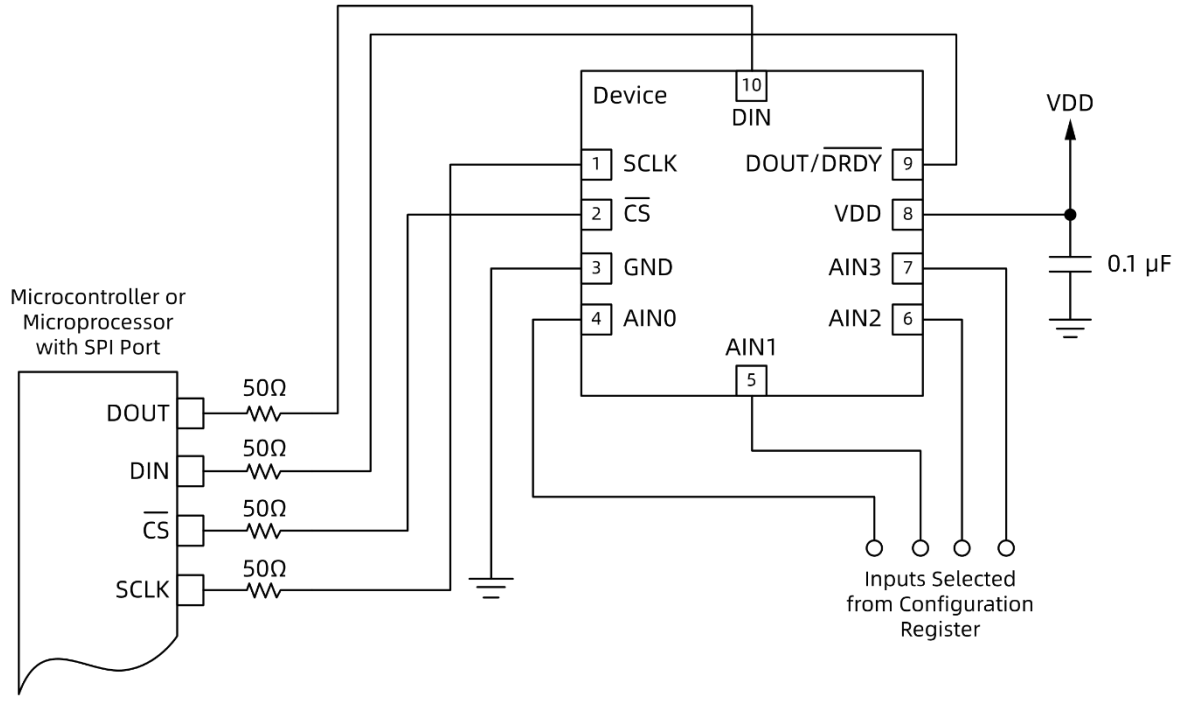


Figure 9. Typical Connections for GD30AD3344

Most microcontroller SPI peripherals can be used with the GD30AD3344. The interface operates in SPI Mode 1, where CPOL = 0 and CPHA = 1. In SPI Mode 1, SCLK idles low and data is initiated or changed only on the rising edge of SCLK; data is latched or read by the master and slave on the falling edge of SCLK. Details can be found in the *SPI Timing Specifications*.

A good practice is to place 50Ω resistors in the series path of each digital pin to provide some short circuit protection. Care must be taken to still meet all SPI timing requirements because these additional series resistors, along with the bus parasitic capacitance present on the digital signal lines, may alter the signal.

The GD30AD3344 are ideal for connecting to differential sources with moderately low source impedance (such as thermocouples and thermistors). Although the GD30AD3344 can read fully differential signals, the device cannot accept negative voltages on either of its inputs due to the ESD protection diodes on each pin. When the inputs exceed the supplies or drop below ground, these diodes turn on to prevent any ESD damage to the device.

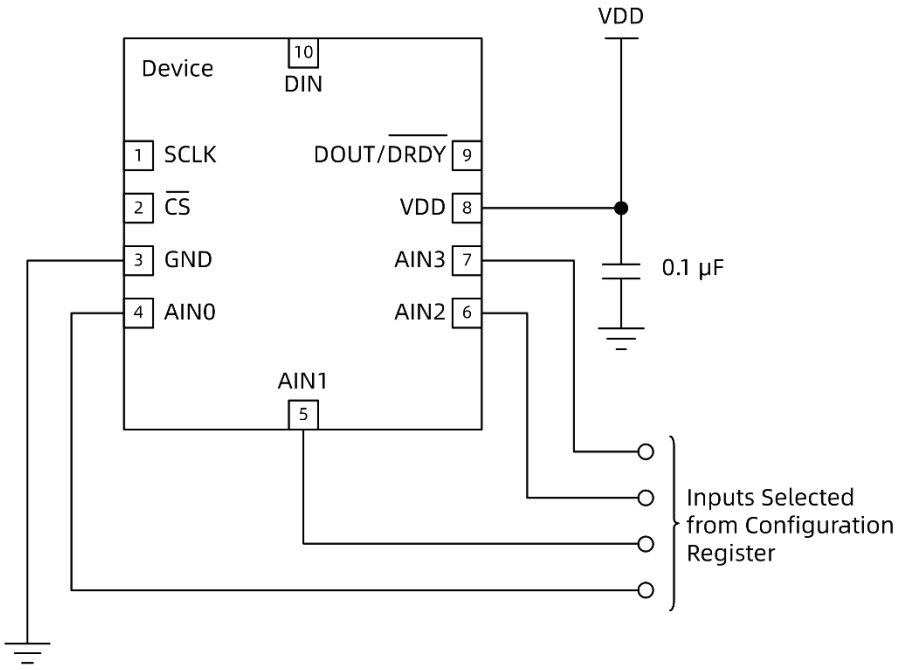
8.2 GPIO Ports for Communication

Most microcontrollers have programmable output (IO) pins that can be set in software as inputs or outputs. If an SPI controller is not available, the GD30AD3344 can be connected to the GPIO pins and the SPI bus pins can simulate the protocol. Use the GPIO pins to generate SPI configured as push or pull inputs or outputs. If the SCLK is low for more than 28 ms, the communication times out. This case means that the GPIO port must be able to provide SCLK pulses with no more than 28 ms between pulses.

8.3 Single-Ended Input

The GD30AD3344 can measure up to four single-ended signals. The GD30AD3344 measures single-ended signals by appropriately configuring the MUX[2:0] bits in the Cofig Register. Figure 10 shows the single-ended connection scheme for the GD30AD3344. The single-ended signal range is from 0V to the positive supply or +FS, whichever is lower. Negative voltages cannot be applied to these devices because the GD30AD3344 can only accept positive voltages relative to ground. The GD30AD3344 does not lose linearity within the input range.

The GD30AD3344 provides a differential input voltage range of ±FSR. The single-ended configuration uses only one-half of the full-scale input voltage range. The differential configuration maximizes the dynamic range of the ADC and provides better common-mode noise rejection than a single-ended configuration.



NOTE: Digital pin connections omitted for clarity.

Figure 10. Measuring Single-Ended Input

The GD30AD3344 also allows AIN3 to be used as a common point for measurements by setting the MUX[2:0] bits appropriately. AIN0, AIN1, and AIN2 can all be measured relative to AIN3. In this configuration, the GD30AD3344 operates with inputs where AIN3 is used as a common point, which increases the usable range allowed.

8.4 Input Protection

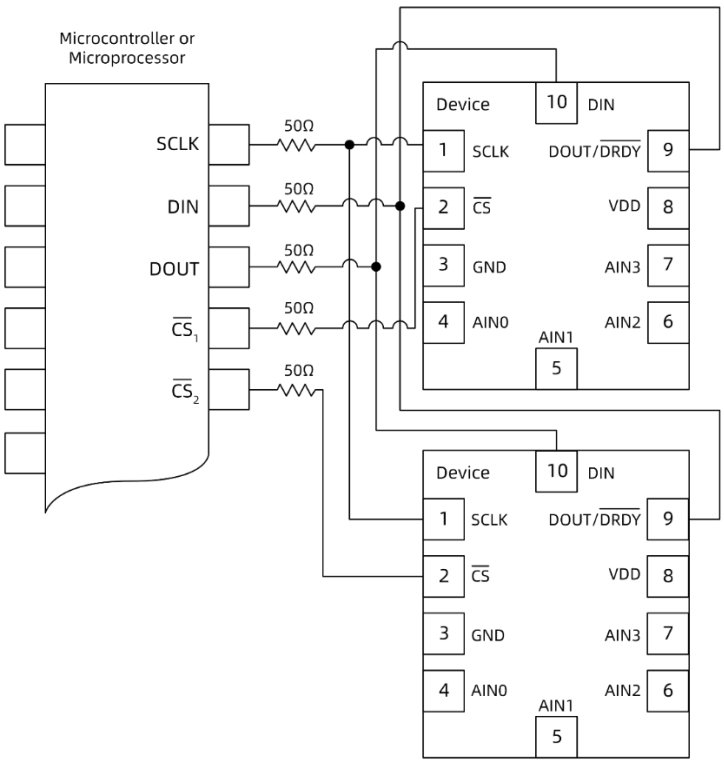
The GD30AD3344 is manufactured using a small footprint, low voltage process. The analog inputs have protection diodes connected to the power rails. However, the current handling capability of these diodes is limited, and the GD30AD3344 may be permanently damaged by analog input voltages exceeding approximately 300mV. One way to prevent overvoltage is to place current limiting resistors on the input lines. The GD30AD3344 analog inputs can withstand up to 10mA of continuous current.

8.5 Unused Inputs and Outputs

Leave unused analog inputs floating or connect unused analog inputs to midsupply or VDD. You can connect unused analog inputs to GND, but higher leakage current may result.

8.6 Connecting Multiple Devices

Connecting multiple GD30AD3344 devices to a single SPI bus, SCLK , DIN, and DOUT/$\overline{\text{DRDY}}$ can be safely shared by using a dedicated chip select ($\overline{\text{CS}}$) for each SPI -capable device . By default, when $\overline{\text{CS}}$ goes high on the GD30AD3344, DOUT/$\overline{\text{DRDY}}$ is pulled up to VDD via a weak pull-up resistor . This feature is designed to prevent DOUT/$\overline{\text{DRDY}}$ from floating near mid-rail and causing excessive current leakage on the microcontroller input. If the PULL_UP_EN bit in the configuration register is set to 0, the DOUT/$\overline{\text{DRDY}}$pin enters tri-state mode when $\overline{\text{CS}}$ transitions high. When $\overline{\text{CS}}$ is high, the GD30AD3344 cannot issue a data-ready pulse on DOUT/$\overline{\text{DRDY}}$. To evaluate when the GD30AD3344 is ready for a new conversion when using multiple devices, the master device can periodically pull $\overline{\text{CS}}$ to low. When $\overline{\text{CS}}$ goes low, the DOUT/$\overline{\text{DRDY}}$ pin is immediately driven high or low. If the DOUT/$\overline{\text{DRDY}}$ line is driven low when $\overline{\text{CS}}$ is low, new data is currently available for clock output at any time. If the DOUT/$\overline{\text{DRDY}}$ line is driven high, no new data is available and the GD30AD3344 returns the last conversion result read. Valid data can be read from the GD30AD3344 at any time without worrying about data corruption.



NOTE: GD30AD3344 power and input connections omitted for clarity.

Figure 11. Connecting Multiple GD30AD3344 Devices

9 Power Supply Recommendations

The device requires a unipolar supply, VDD, to power the analog and digital circuits of the device.

9.1 Power Supply Timing

After VDD stabilizes before communicating with the device to complete the power-on reset process.

9.2 Power Supply Decoupling

Good power supply decoupling is important to achieve optimal performance. VDD must be decoupled using at least a 0.1 µF capacitor as shown in Figure 12. The 0.1 µF bypass capacitor provides the instantaneous burst of additional current required from the power supply when the device is switching. Place the bypass capacitor as close to the device's power pins as possible using low impedance connections. Use multilayer ceramic chip capacitors (MLCCs) with low equivalent series resistance (ESR) and inductance (ESL) characteristics for power supply decoupling. For very sensitive systems or systems in harsh noisy environments, avoid using vias to connect capacitors to device pins to improve noise immunity. If vias must be used to connect capacitors to device pins, it is recommended to use multiple vias in parallel to reduce the overall inductance.

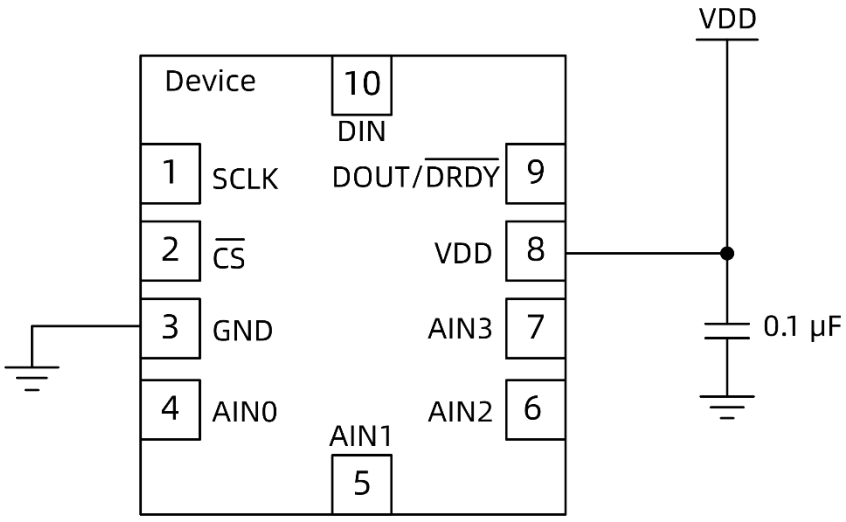


Figure 12. GD30AD3344 Power Supply Decoupling

10 Layout

10.1 Layout Guide

Employ best design practices when laying out the printed circuit board (PCB) for analog and digital components. For optimal performance, separate analog components [such as ADCs, amplifiers, references, digital-to-analog converters (DACs), and analog MUXs] from digital components [such as microcontrollers, complex programmable logic devices (CPLDs), field programmable gate arrays (FPGAs), radio frequency (RF) transceivers, universal serial bus (USB) transceivers, and switching regulators]. Figure 13 shows an example of good component placement. While Figure 13 provides a good example of component placement, the optimal placement for each application depends on the geometry, components, and PCB manufacturing capabilities employed. That said, no one layout will work perfectly for every design, and careful consideration must always be used when designing with any analog component.

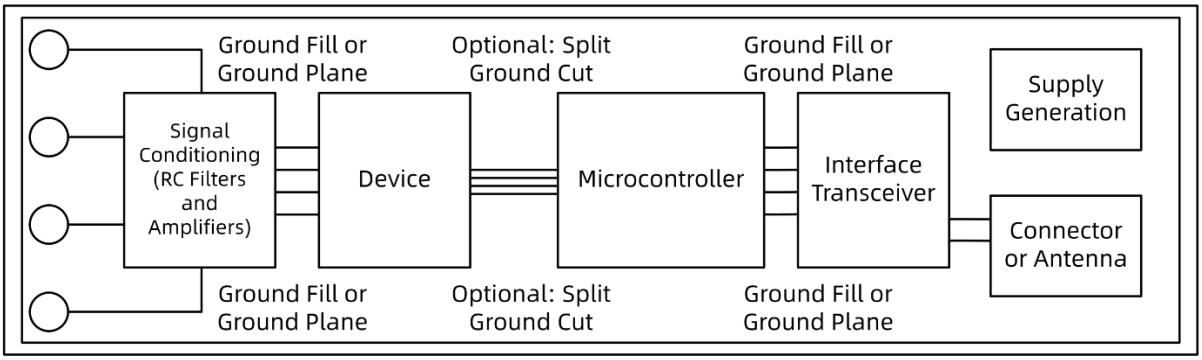


Figure 13. System Component Placement

Outlined below are some basic recommendations for the GD30AD3344 layout to get the best performance from the ADC. A good design can be ruined by poor circuit layout.

Separate analog and digital signals. First, divide the board into analog and digital sections as the layout allows. Keep digital lines away from analog lines. This prevents digital noise from coupling back into the analog signals.

Fill empty areas on signal layers with ground.

Provide a good ground return path. Signal return current flows on the path of least impedance. If the ground plane is cut or there are other traces preventing current from flowing next to the signal trace, it must find another path to return to the source and complete the circuit. If it is forced into a larger path, it increases the chance of signal radiation. Sensitive signals are more susceptible to EMI interference.

Use bypass capacitors on the power supplies to reduce high frequency noise. Do not place vias between the bypass capacitors and active devices. Placing bypass capacitors on the same layer close to active devices yields the best results.

Consider the resistance and inductance of the wiring. In general, the resistance of the input trace reacts with the input bias current and causes additional error voltage. Reduce the loop area enclosed by the source signal and return current to reduce the inductance in the path. Reduce inductance to reduce EMI pickup and reduce the high-frequency impedance seen by the device.

The two inputs going into the measurement source must be matched differential inputs.

Analog inputs with differential connections must place a capacitor at the input differentially. The best input combination for differential measurements uses adjacent analog input lines, such as AIN0, AIN1 and AIN2, AIN3. The differential capacitor must be of high quality. The best ceramic chip capacitor is C0G (NPO), which has stable characteristics and low noise characteristics.

10.2 Layout Examples

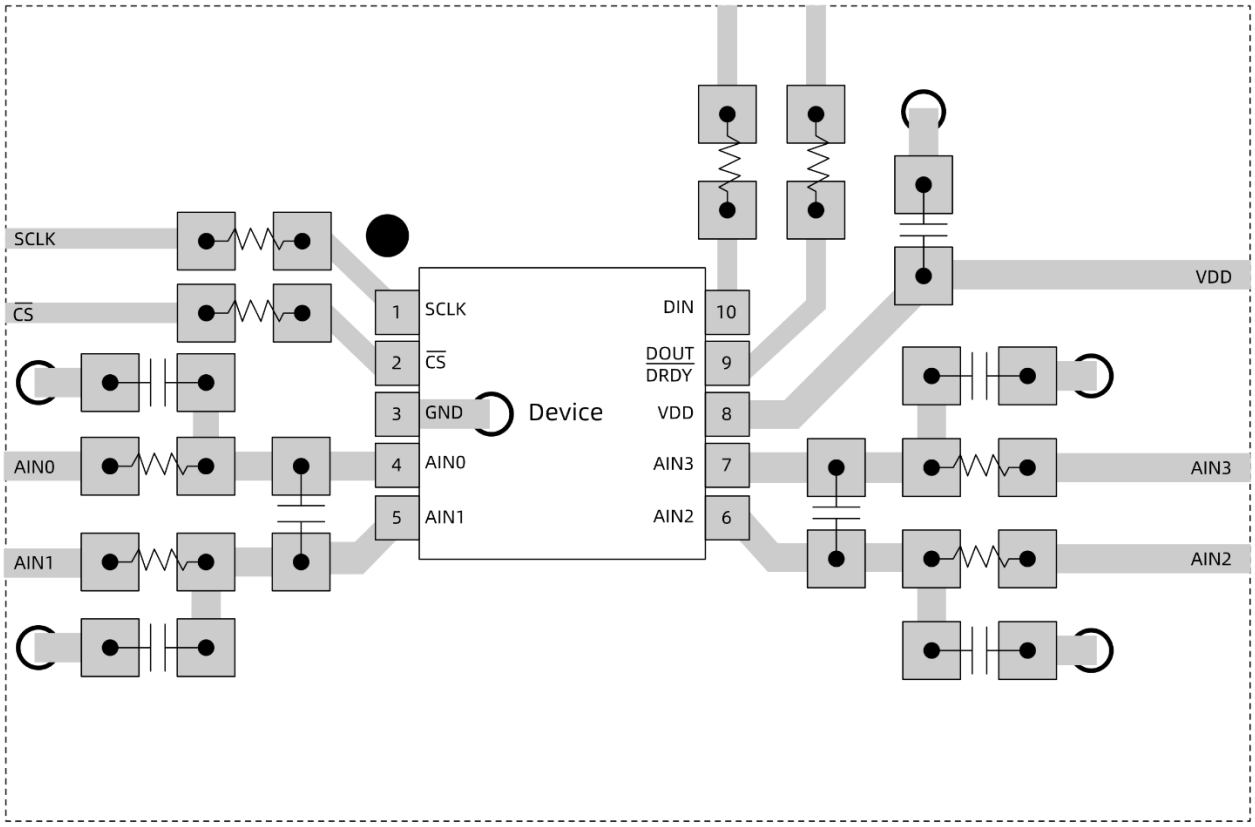
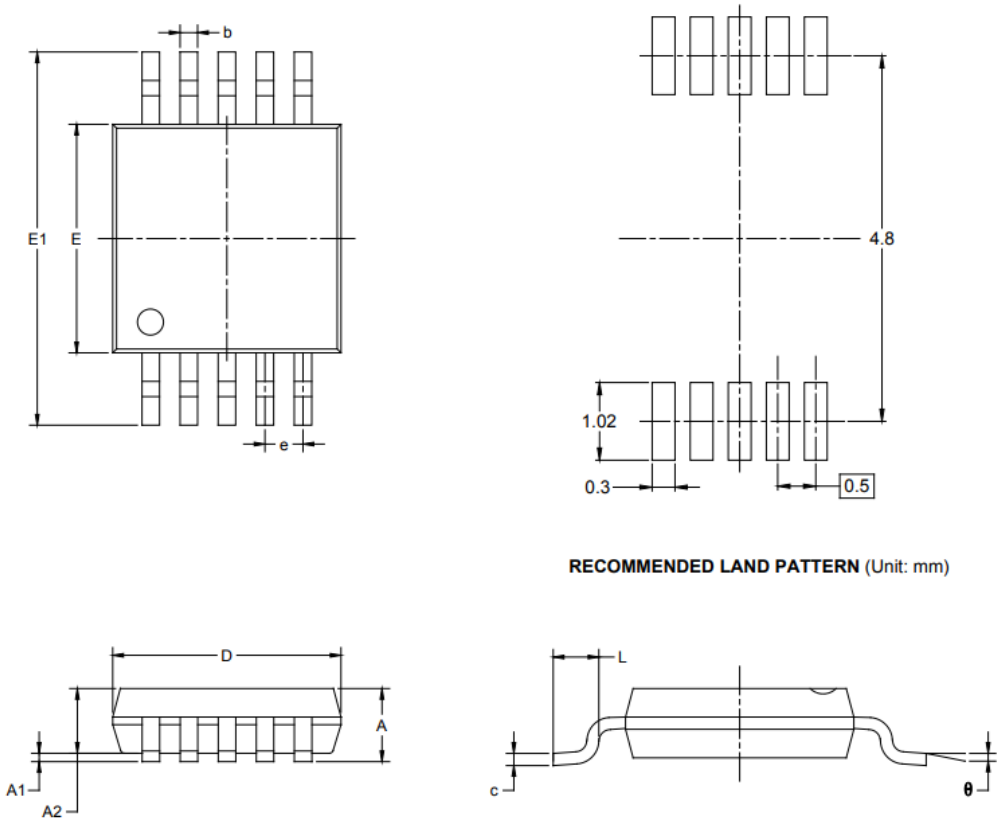


Figure 14. GD30AD3344 MSOP-10 Package

11 Package Information

11.1 Outline Dimensions

MSOP-10 Package



Note:

1. All dimensions are in millimeters.
2. Package dimensions does not include mold flash, protrusions, or gate burrs.
3. Refer to Table 9. *MSOP-10 Dimensions (mm).*

Table 9. MSOP-10 Dimensions (mm)

SYMBOL	MIN	NOM	MAX
A	0.820		1.100
A1	0.020		0.150
A2	0.750		0.950
b	0.180		0.280
c	0.090		0.230
D	2.900		3.100
E	2.900		3.100
E1	4.750		5.050
e	0.500 BSC		
L	0.400		0.800
θ	0°		6°

12 Ordering Information

Ordering Code	Package Type	ECO Plan	Packing Type	MOQ	OP Temp(°C)
GD30AD3344AMTR-I	MSOP10	Green	Reel	3000	−40°C to +125°C

13 Revision History

REVISION NUMBER	DESCRIPTION	DATE
1.0	Initial release and device details	2024

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