# 36V General-Purpose Industry Comparators

## 1 Features

- Wide Supply: 3.0V to 36V
- Faster Response Time: 1.3us (typical)
- Low Offset Voltage: ±2mV (typical)
- Low Input Bias Current: 25nA(typical)
- Large Voltage Gain: 100 dB (typical)
- Open Collector Output
- Input Common-Mode Voltage Range Includes Ground
- Differential Input Voltage Range Equal To Power Supply
- Extended Temperature Range: -40°C to +125°C

## 2 Applications

- Industrial Application
- Solar Inverter
- White Goods
- Battery Management System
- Medical Equipment

## 3 Description

The GD30CP2903/2901 are dual and quad channel voltage comparators with very low input offset voltage specifcaton. They are designed to operate from a single power supply over a wide range of voltages, however operation from split power supplies is also possible. They offer low power supply current independent of the magnitude of the power supply voltage.

These comparators family are designed to directly interface with TTL and CMOS. When operating from both plus and minus power supplies, the comparators could directly interface with MOS logic where their low power drain is a distinct advantage over standard comparators.

The GD30CP2903(dual) is offered in SOIC-8L and MSOP-8L packages, the quad of GD30CP2901 is offered in SOIC-14L and TSSOP-14L packages.

**Device Information**[1]

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| GD30CP2903 | SOIC-8L | 4.90mm x 3.92mm |
| | MSOP-8L | 3.00mm x 3.00mm |
| GD30CP2901 | SOIC-14L | 8.73mm x 3.95mm |
| | TSSOP-14L | 4.96mm x 4.40mm |

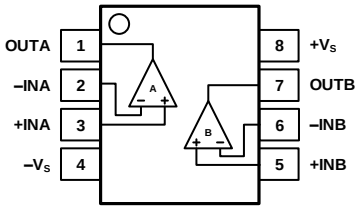
1. For packaging details, see *Package Information* section.

# Table of Contents

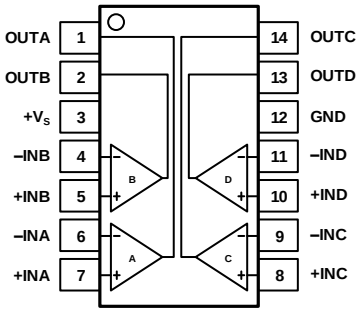
# 4 Device Overview

## 4.1 Pinout and Pin Assignment

GD30CP2903
SOIC-8L / MSOP-8L
Top View




GD30CP2901
SOIC-14L / TSSOP-14L
Top View




## 4.2 Pin Description

| NAME | PIN TYPE[1] | FUNCTION |
|---|---|---|
| -IN | I | Inverting input of the comparator. The voltage range is from ($V_{S-}$–V) to ($V_{S+}$ + 20V). |
| +IN | I | Non-inverting input of the comparator. This pin has the same voltage range as –IN. |
| $+V_S$ | P | Positive power supply. The voltage is from 3.0V to 36V. Split supplies are possible as long as the voltage between $V_{S+}$ and $V_{S-}$ is from 3.0V to 36V. |
| $-V_S$ | P | Negative power supply. It is normally tied to ground. It can also be tied to a voltage other than ground as long as the voltage between $V_{S+}$ and $V_{S-}$ is from 3.0V to 36V. |
| OUT | O | Comparator output. |

1. I = Input, O = Output, P = Power.

# 5 Parameter Information

## 5.1 Absolute Maximum Ratings

Exceeding the operating temperature range (unless otherwise noted)[1]

| SYMBOL | PARAMETER | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_{S+}$ to $V_{S-}$ | Supply Voltage | | 40 | V |
| $V_I$ | Differential Input Voltage | −36 | 36 | V |
| $I_I$ | Signal Input Voltage Range | −0.3 | 40 | V |
| | Output Short-Circuit | Continuous | | s |
| $T_J$ | Junction Temperature | | 150 | °C |
| $T_A$ | Operate Temperature Range | −40 | 125 | °C |
| $T_{stg}$ | Storage Temperature Range | −65 | +150 | °C |
| | Lead Temperature Range (Soldering 10 sec) | | 260 | °C |

1. The maximum ratings are the limits to which the device can be subjected without permanently damaging the device. Note that the device is not guaranteed to operate properly at the maximum ratings. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

## 5.2 Recommended Operation Conditions

| SYMBOL[1,2] | PARAMETER | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $V_S$ | Input supply voltage range | 3.0 | | 36 | V |
| $V_{CM}$ | $V_S$ = 5.0V to 36V | $-V_S$ | | $+V_S$ - 1.5 | V |
| | $V_S$ = 5.0V to 36V, $T_A$ =− 40°C to 125°C | $-V_S$ | | $+V_S$ – 2.0 | |
| $T_A$ | Operating temperature range | −40 | | 125 | °C |

1. The device is not guaranteed to function outside of its operating conditions.

## 5.3 Electrical Sensitivity

| SYMBOL | CONDITIONS | VALUE | UNIT |
|---|---|---|---|
| $V_{ESD(HBM)}$ | Human-body model (HBM), ANSI/ESDA/JEDEC JS-001-2017[1] | ±500 | V |
| $V_{ESD(CDM)}$ | Charge-device model (CDM), ANSI/ESDA/JEDEC JS-002-2022[2] | ±1000 | V |

1. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
2. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 5.4 Thermal Characteristics

| SYMBOL[1] | CONDITIONS | PACKAGE | VALUE | UNIT |
|---|---|---|---|---|
| $\Theta_{JA}$ | Package Thermal Resistance | MSOP-8L | 171 | °C/W |
| | | SOIC-8L | 124.7 | |
| | | TSSOP-14L | 135.8 | |
| | | SOIC-14L | 160.9 | |

1. Thermal characteristics are based on simulation, and meet JEDEC document JESD51-7.

## 5.5 Electrical Characteristics

$V_S$ = 5.0 V to 36V, $T_A$ = +25°C, unless otherwise noted. Boldface limits apply over the specified temperature range.

| SYMBOL | PARAMETER | CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| | | | | | | |
| $V_{OS}$ | Input offset voltage | $V_S$ = 5.0 V to 30 V, $V_{OUT}$ = 1.4 V | | ±2 | ±7 | mV |
| | | $V_S$ = 5.0 V to 30 V, $V_{OUT}$ = 1.4 V<br>$T_A$ = −40 to +125°C | | | ±15 | |
| **INPUT BIAS CURRENT** | | | | | | |
| $I_B$ | Input bias current | $V_{CM}$ = 0 | | −25 | −250 | nA |
| | | $V_{CM}$ = 0,$T_A$ = −40 to +125°C | | | −400 | |
| $I_{OS}$ | Input offset current | $V_{CM}$ = 0 | | 5 | 50 | nA |
| | | $V_{CM}$ = 0,$T_A$ = −40 to +125°C | | | 200 | |
| **INPUT VOLTAGE** | | | | | | |
| $V_{CM}$ | Common-mode voltage range | $V_S$ = 5.0 V to 36 V, | $-V_S$ | | $+V_S$ - 1.5 | V |
| | | $V_S$ = 5.0 V to 36 V<br>$T_A$ = −40 to +125°C | $-V_S$ | | $+V_S$ – 2.0 | |
| **VOLTAGE GAIN** | | | | | | |
| $A_{VD}$ | Large-signal differential-voltage amplification | $V_{CC}$ = 15 V, $V_{OUT}$ = 1 V to 11 V<br>$R_L$ ≥ 15KΩ | 50 | 200 | | V/mV |
| **PROPAGATION DELAY TIME** | | | | | | |
| $T_{PD}$ | Propagation delay time | $R_L$ = 5.1KΩ, $V_{RL}$ = 5 V, $C_L$ = 15 pF<br>TTL-Level Input Step | | 0.3 | | µs |
| | | $R_L$ = 5.1KΩ, $V_{RL}$ = 5 V, $C_L$ = 15 pF<br>100mV Input Step With 5mV Overdrive | | 1.3 | | |
| **OUTPUT** | | | | | | |
| $V_{OL}$ | Low output voltage swing | $I_{OL}$ = 4mA, $V_{ID}$ =−1V | | 200 | 400 | mV |
| | | $I_{OL}$ = 4mA, $V_{ID}$ =-1V<br>$T_A$ = −40 to +125°C | | | 700 | |
| $I_{OL}$ | Low-level output current | $V_{OL}$ = 1.5V, $V_{ID}$ = 1V | | 6 | 16 | mA |
| $I_{OH}$ | High-level output current | $V_{OL}$ = 5 V, $V_{ID}$ = 1V | 0.1 | 50 | | nA |
| | | $V_{OL}$ = 30 V, $V_{ID}$ = 1V<br>$T_A$ = −40 to +125°C | | | 1 | µA |
| **POWER SUPPLY** | | | | | | |
| $V_S$ | Operating supply voltage | $T_A$ = −40°C to +125°C | 3.0 | | 36 | V |
| $I_Q$ | Quiescent current of GD30CP2903 | $V_S$ = 5 V | | 400 | 1000 | µA |
| | | $V_S$ = 30 V | | 650 | 1750 | |
| $I_Q$ | Quiescent current of GD30CP2901 | $V_S$ = 5 V | | 850 | 1990 | µA |
| | | $V_S$ = 30 V | | 1150 | 2490 | |

1. Guaranteed by design and engineering sample characterization.

## 5.6 Typical Characteristics

$V_S$ = 5V, $R_L$ = 5.1kΩ $T_A$ = +25°C, unless otherwise noted.

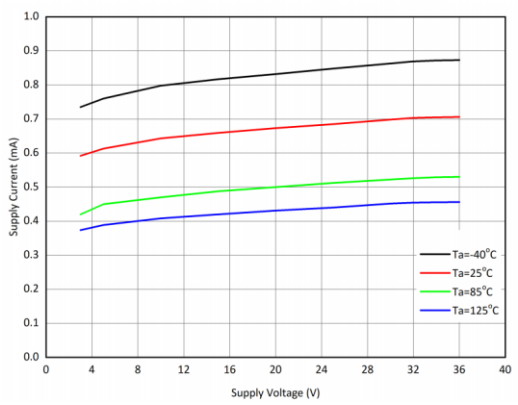



**Figure 1. LTA903L Quiescent Current vs. Supply Voltage**

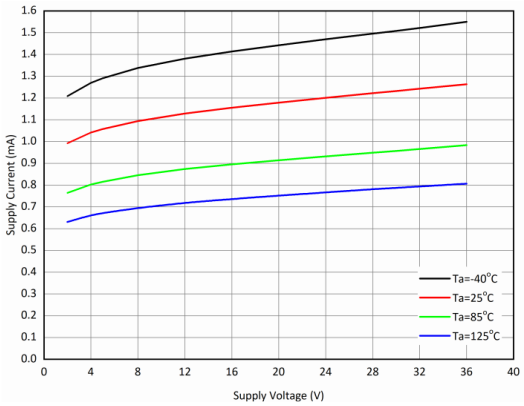



**Figure 2. LTA901L Quiescent Current vs. Supply Voltage**

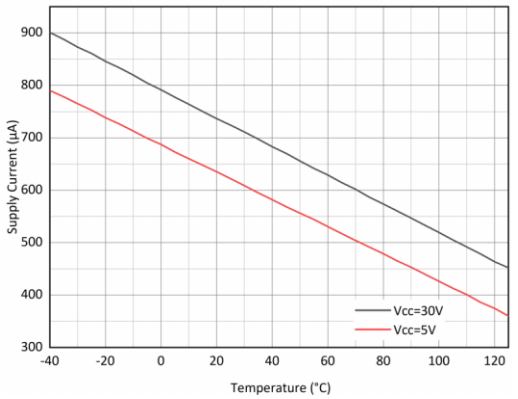



**Figure 3. LTA903L Quiescent Current vs. Temperature**

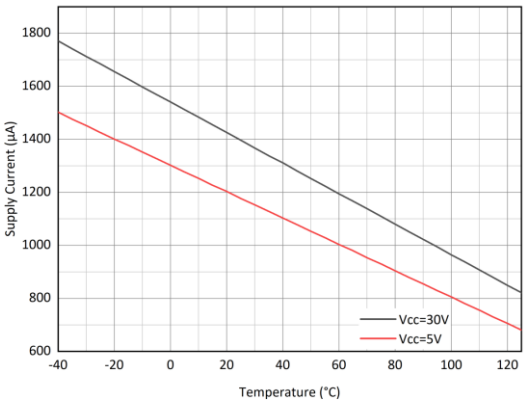



**Figure 4. LTA901L Quiescent Current vs. Temperature**

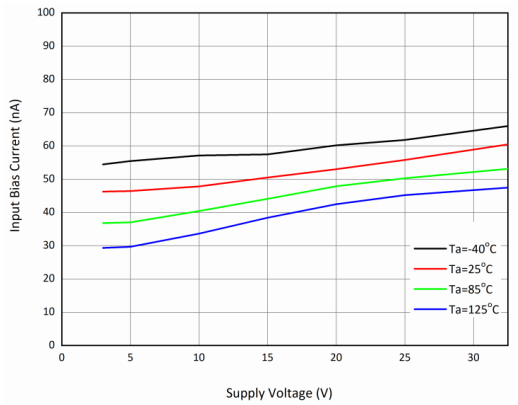



**Figure 5. Input Bias Current vs. Supply Voltage**

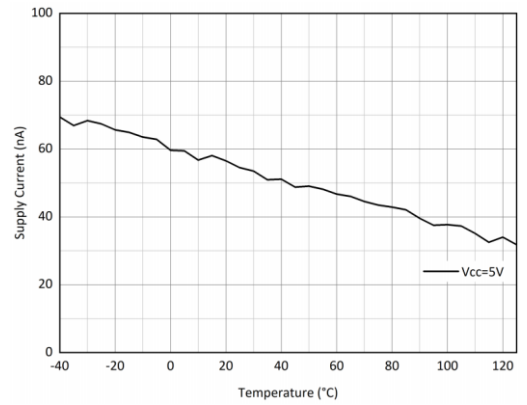



**Figure 6. Input Bias Current vs. Supply Temperature**

## Typical Characteristics (continued)

$V_{IN}$ = 5V, $V_{OUT}$ = 3.3V, L = 2.2uH, $T_A$ = 25°C, unless otherwise noted.

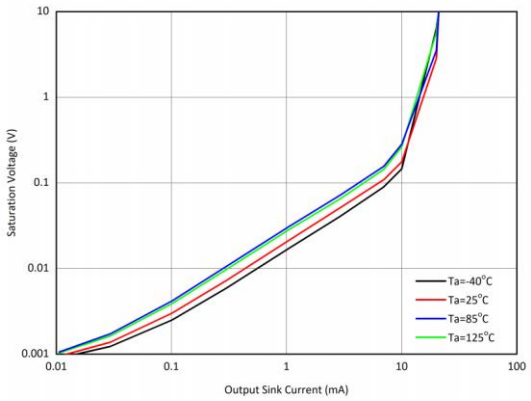



**Figure 7. Output Sink Curent vs. Saturaton Voltage**

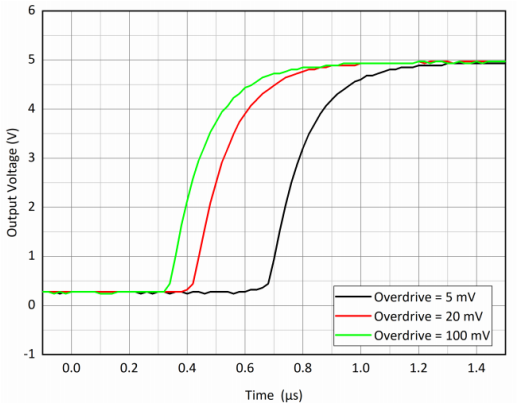



**Figure 8. Response Time for Various Over Drivs Positve Transition**

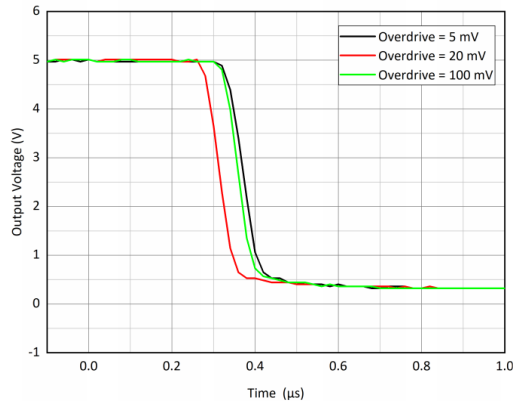
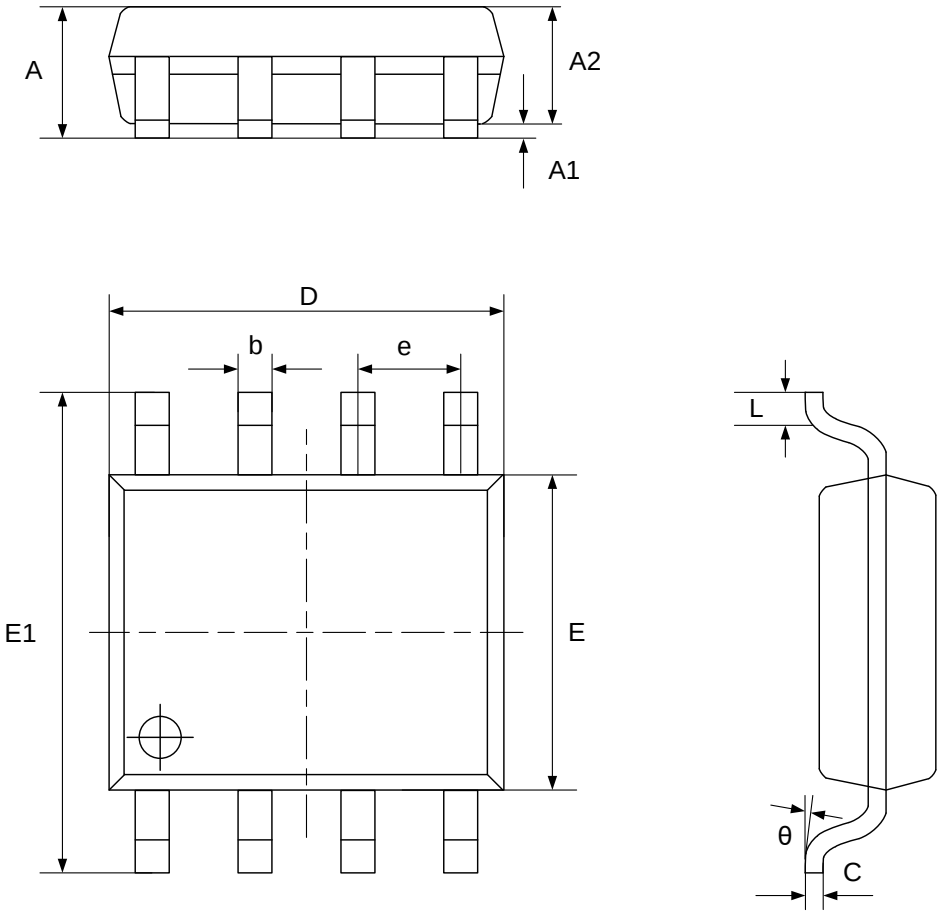



**Figure 9. Response Time for Various Over Drivs Negative Transition**

# 6 Package Information

## 6.1 Outline Dimensions

### SOIC-8L Package Outline



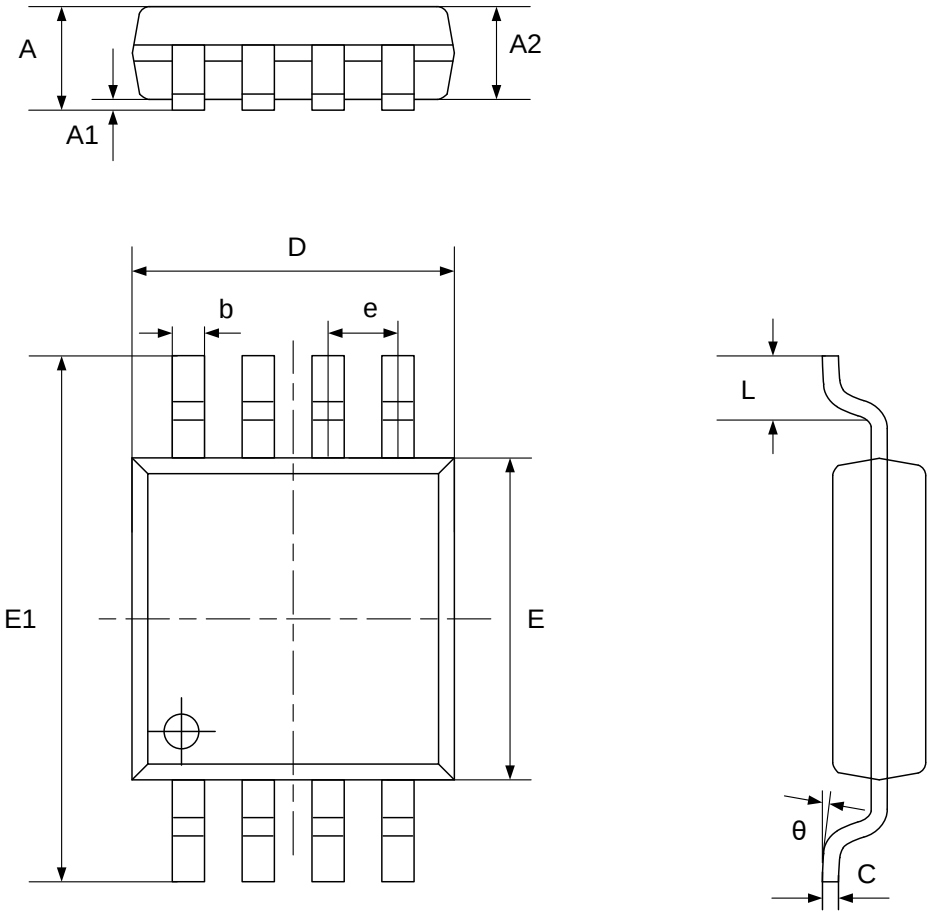

NOTES: (continued)

1. Refer to the Table 1. *SOIC-8L dimensions(mm)*.

**Table 1. SOIC-8L dimensions(mm)**

| SYMBOL | MIN | NOM | MAX |
|---|---|---|---|
| A | 1.370 | | 1.670 |
| A1 | 0.070 | | 0.170 |
| A2 | 1.300 | | 1.500 |
| b | 0.306 | | 0.506 |
| C | | 0.203 | |
| D | 4.700 | | 5.100 |
| E | 3.820 | | 4.020 |
| E1 | 5.800 | | 6.200 |
| e | | 1.270 | |
| L | 0.450 | | 0.750 |
| θ | 0° | | 8° |

## MSOP-8L Package Outline



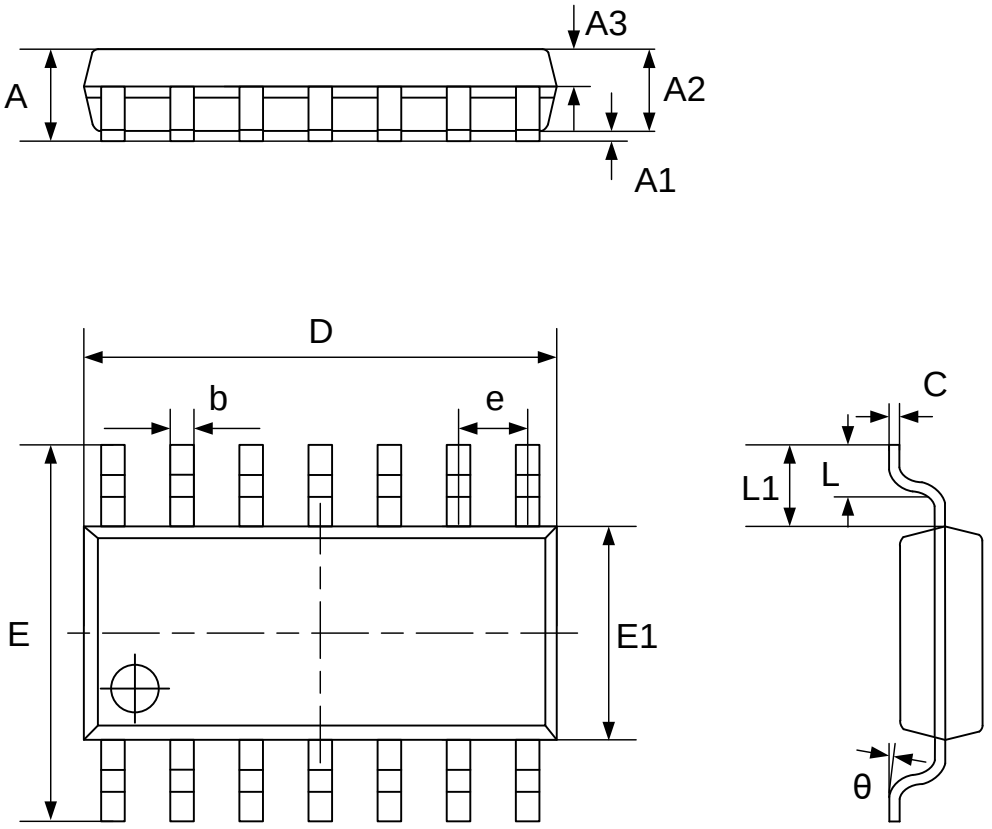

NOTES: (continued)

1. Refer to the Table 2. *MSOP-8L dimensions(mm)*.

**Table 2. MSOP-8L dimensions(mm)**

| SYMBOL | MIN | NOM | MAX |
|---|---|---|---|
| A | 0.800 | | 1.100 |
| A1 | 0.050 | | 0.150 |
| A2 | 0.750 | | 0.950 |
| b | 0.290 | | 0.380 |
| C | 0.150 | | 0.200 |
| D | 2.900 | | 3.100 |
| E | 2.900 | | 3.100 |
| E1 | 4.700 | | 5.100 |
| e | | 0.650 | |
| L | 0.400 | | 0.700 |
| θ | 0° | | 8° |

## SOIC-14L Package Outline



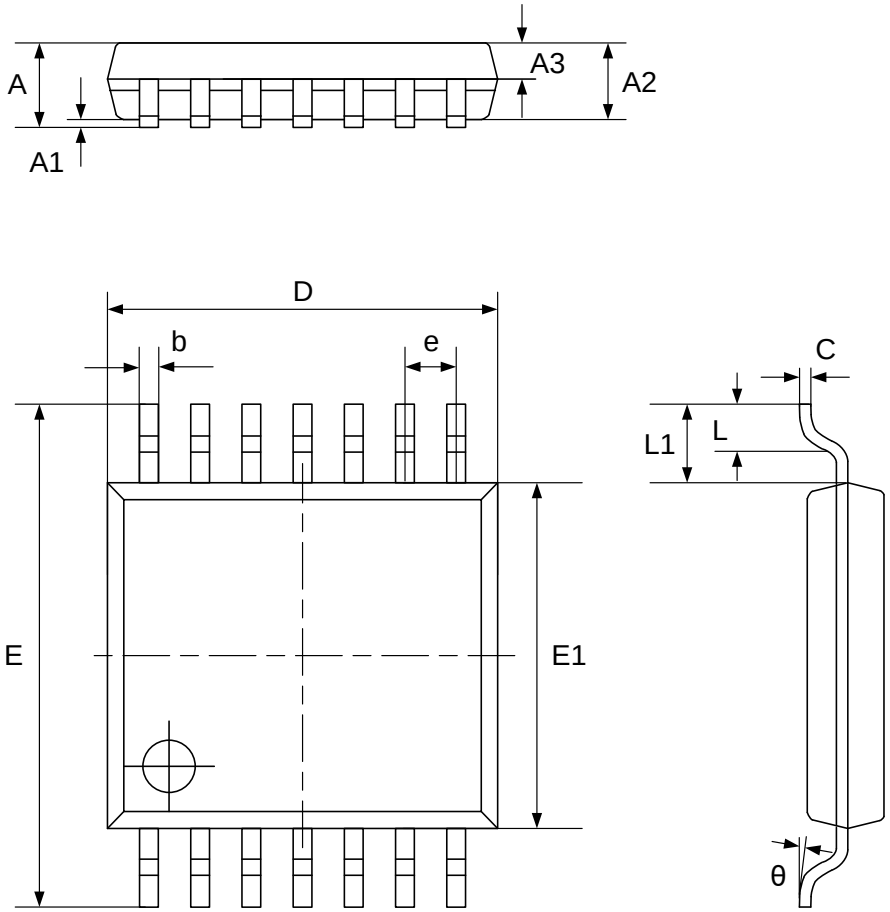

NOTES: (continued)

1. Refer to the *Table 3. SOIC-14L dimensions.*

**Table 3. SOIC-14L dimensions**

| SYMBOL | MIN | TYP | MAX |
|---|---|---|---|
| A | 1.450 | | 1.850 |
| A1 | 0.100 | | 0.300 |
| A2 | 1.350 | | 1.550 |
| A3 | 0.550 | | 0.750 |
| b | | 0.406 | |
| C | | 0.203 | |
| D | 8.630 | | 8.830 |
| E | 5.840 | | 6.240 |
| E1 | 3.850 | | 4.050 |
| e | | 1.270 | |
| L1 | 1.040 REF | | |
| L | 0.350 | | 0.750 |
| θ | 2° | | 8° |

## TSSOP-14L Package Outline




NOTES: (continued)

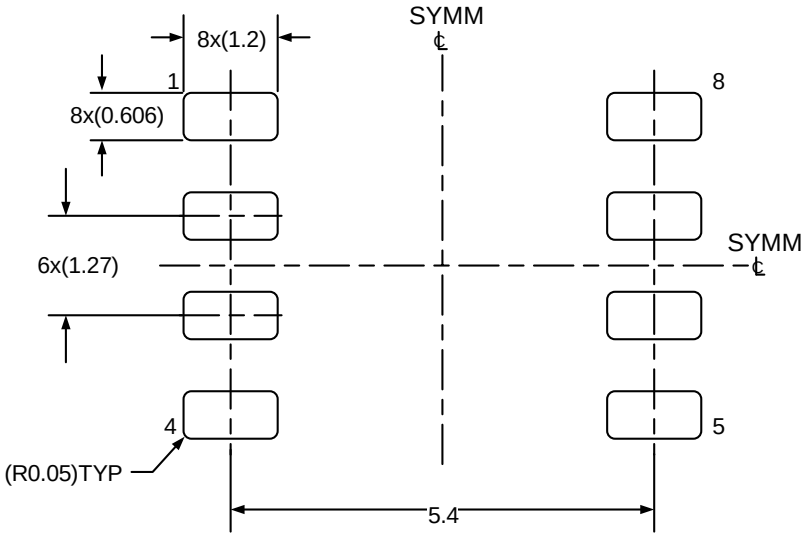
1. Refer to the *Table 4. TSSOP-14L dimensions*

**Table 4. TSSOP-14L dimensions**

| SYMBOL | MIN | TYP | MAX |
|---|---|---|---|
| A | | | 1.200 |
| A1 | 0.050 | | 0.150 |
| A2 | 0.900 | | 1.050 |
| A3 | 0.390 | | 0.490 |
| b | 0.200 | | 0.290 |
| C | 0.130 | | 0.180 |
| D | 4.860 | | 5.060 |
| E | 6.200 | | 6.600 |
| E1 | 4.300 | | 4.500 |
| e | | 0.650 | |
| L1 | 1.000 REF | | |
| L | 0.450 | | 0.750 |
| θ | 0° | | 8° |

## 6.2 Recommended Land Pattern

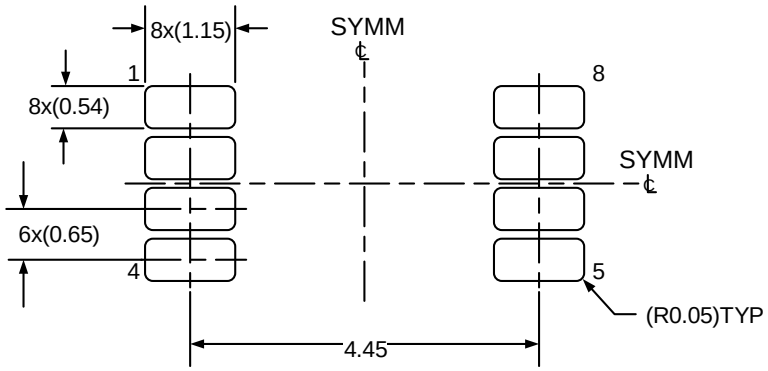
**SOIC-8L Land Pattern Example**




NOTES:

1. Refer to the IPC-7351 can also help you complete the designs.
2. Exposed metal shown.
3. Drawing is 10X scale.

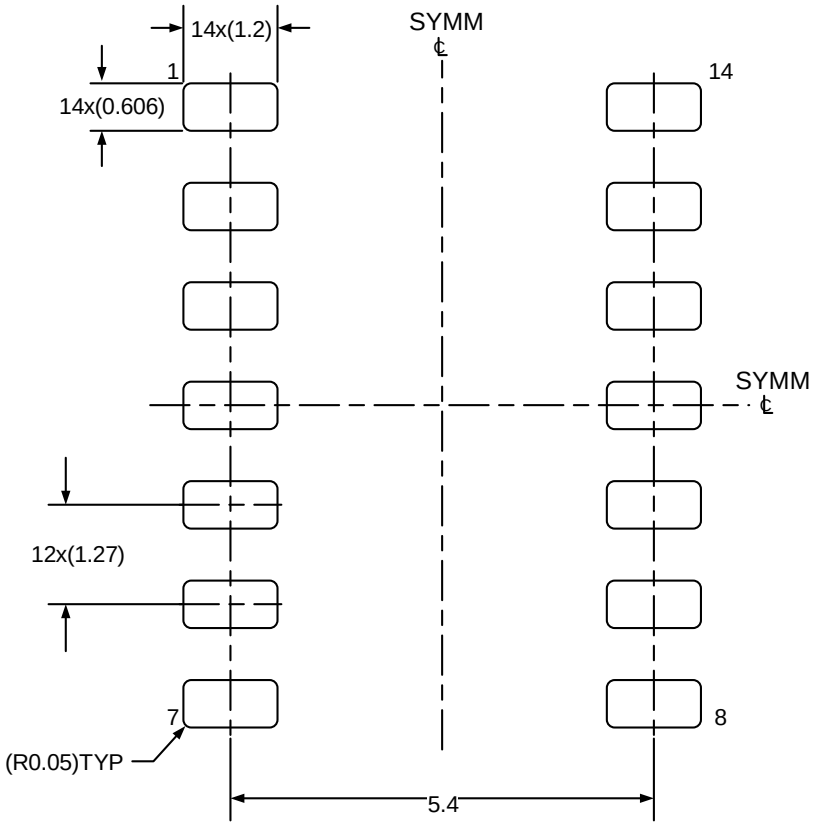
## MSOP-8L Land Pattern Example




NOTES: (continued)

1. Refer to the IPC-7351 can also help you complete the designs.
2. Exposed metal shown.
3. Drawing is 10X scale.

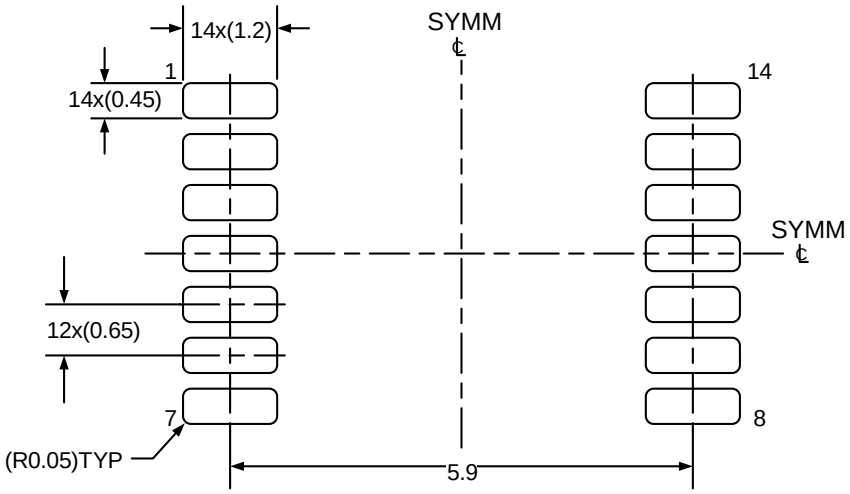
## SOIC-14L Land Pattern Example




NOTES: (continued)

1. Refer to the IPC-7351 can also help you complete the designs.
2. Exposed metal shown.
3. Drawing is 10X scale.

## TSSOP-14L Land Pattern Example




NOTES: (continued)

1. Refer to the IPC-7351 can also help you complete the designs.
2. Exposed metal shown.
3. Drawing is 10X scale.

# 7 Ordering Information

| Ordering Code | Package Type | ECO Plan | Packing Type | MOQ | OP Temp(°C) |
|---|---|---|---|---|---|
| GD30CP2903WMTR-IL2 | MSOP-8L | Green | Tape & Reel | 3000 | −40°C to +125°C |
| GD30CP2903WLTR-IL2 | SOIC-8L | Green | Tape & Reel | 4000 | −40°C to +125°C |
| GD30CP2901ZLTR-IL4 | SOIC-14L | Green | Tape & Reel | 2500 | −40°C to +125°C |
| GD30CP2901ZPTR-IL4 | TSSOP-14L | Green | Tape & Reel | 3000 | −40°C to +125°C |

# 8 Revision History

| REVISION NUMBER | DESCRIPTION | DATE |
|---|---|---|
| 1.0 | Initial release and device details | 2024 |

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